UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,309	12/15/2001	Gary Smith	111215REJ.US	2338

7590 10/17/2005

ROBERT E. KREBS, ESQ
THELEN REID 7 PRIEST LLP
P.O. BOX 640640
SAN JOSE, CA 95164-0640

EXAMINER	
AGHDAM, FRESHTEH N	
ART UNIT	**PAPER NUMBER**
2631	

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,309	SMITH, GARY	
	Examiner	Art Unit	
	Freshteh N. Aghdam	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☒ Claim(s) *9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments, filed 7/28/2005, with respect to the rejection(s) of claim(s) 1-10 under the instant application's disclosed prior art, Horner et al, Stevenson, Jaffe, and Blatus have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Kerth et al (US 6,804,497), Tapio (US 2002/0105378), Baltus et al (US 5,808,509), and Horner et al (US 5,357,544).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kerth et al (US 6,804,497), and further in view of Stevenson (US 6,674,812).

As to claims 1 and 3, Kerth teaches a digital intermediate frequency down-conversion circuitry for down converting in-phase and quadrature signal components of a digitized communication signal comprising: processing a single serial digital bit stream formed of the in-phase and quadrature signal components of the digitized communication signal logically to produce a digital representation of down converted in-

phase and quadrature compronents; and recombining the digital representation of the down converted in-phase and quadrature components with a reconstruction filter in a manner to obtain a baseband signal substantially free of image artifacts (Fig. 4; Col. 8, Lines 24- Col. 9, Line21). Kerth is silent about processing the digital in-phase and quadrature signals through a set of simple logic to produce digital representation of downconverted in-phase and quadrature components. One of ordinary skill in the art would clearly recognize that digital signals are processed logically and use of logic elements such as AND, OR, XOR, XNOR gates to mix and/or combine digital bits are well known in the art as evidenced by Stevenson see (Col. 9, Lines 55-57). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Stevenson with Kerth in order to use logic elements such as AND, OR, XOR, XNOR gates to mix and/or combine digital bits to function in desirable manner.

Claims 2 and 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kerth et al and Stevenson, further in view of Horner et al (US 5,357,544), and Baltus (US 5,808,509).

As to claims 2 and 4-5, Kerth teaches generating a reference signal as a sine wave (Fig. 4). One of ordinary skill in the art would clearly recognize that since the reference signal is mixed with the digitized in-phase and quadrature components according to a clock signal (Fig. 2; Col. 5, Lines 4-20); therefore, it is a sine wave. Kerth and Stevenson teach recombining digitally the in-phase and quadrature signals to obtain a digitally combined signal (Fig. 4, means 436 is a IIR or FIR). Kerth is silent about employing an oversampled digital word of four bits in length from a source digital

oscillator as a reference signal to achieve at least sixteen levels of accuracy as a sine wave and binary weighting the combined signal into a digital reconstruction filter to produce a downconverted signal that is unaffected by resistor tolerance. Horner teaches the reference signal generator 24 that is a periodic oversampled digital word generated from a 128 point cosine wave stored in the cosine table 28 by taking eight entries spaced sixteen points (Fig. 2; Col. 4, Lines 55-65). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Horner with Kerth and Stevenson in order to obtain or achieve the desired resolution (Col. 4, Lines 60-64). Baltus teaches binary weighting by applying resistor means to the filtered down converted signal and producing Intermediate Frequency signals IF1-IF4 (Fig. 3; Col. 3, Lines 32-43). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Baltus with Kerth, Stevenson, and Horner in order to binary weighting the combined signal for forming the intermediate frequency signals IF1-IF4 to provide an accurate quadrature receiver that is low cost and has reduced power consumption (Col. 1, Lines 38-40).

Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tapio (US 2002/0105378), and further in view of Stevenson.

As to claim 6, Tapio teaches performing down conversion to produce analog I and Q signal: oversampling the analog signal to obtain an oversampled digital signal (Fig. 6, means 71 and 72); producing a periodic oversampled digital reference signal (Fig. 9, means DDS CARRIER); and combining the digital signal with the digtal reference signal to produce an image cancelled digital baseband signal (Fig. 9; Par. 16-

18). Tapio is silent about logically combining the digital signal with the digtal reference signal. One of ordinary skill in the art would clearly recognize that digital signals are combined logically and use of logic elements such as AND, OR, XOR, XNOR gates to mix and/or combine digital bits are well known in the art as evidenced by Stevenson see (Col. 9, Lines 55-57). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Stevenson with Tapio in order to use logic elements such as AND, OR, XOR, XNOR gates to mix and/or combine digital bits to function in desirable manner.

As to claim 7, Tapio teaches converting the digital baseband signal to an analog baseband signal (Fig. 3, means 1 and 3).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kerth et al, further in view of Stevenson and Baltus et al.

As to claim 8, Kerth teaches a first frequency down-conversion circuit employing a first local oscillator (Fig. 2 and 4, means 222, 409) for down-converting in-phase and quadrature signal components of a communication signal to a first intermediate frequency; ADC (analog to digital converter) for generating an in-phase and quadrature bits streams (Fig. 4, means 418, 421); a digital I and Q down-converter (Fig. 4, means 427 and 430) down-converts the digital one bit streams I and Q into a down-converted in-phase and quadrature signals; and reconstruction filter is coupled to a digital down-converter to recover in-phase and quadrature signals from the down-converted in-phase and quadrature components substantially free of image artifacts (Col. 8, Lines 24- Col. 9, Line21). One of ordinary skill in the art would clearly recognize that it is well known in

the art to down-convert and baseband in-phase and quadrature signal in one step. One of ordinary skill in the art would clearly recognize that in order to down covert the digital I and Q signals, a digital oscillator could be used to be mixed with the digital I and Q signals. Kerth is silent about a mixing circuitry that employs a set of logic gates. One of ordinary skill in the art would clearly recognize that digital signals are processed logically and use of logic elements such as AND, OR, XOR, XNOR gates to mix and/or combine digital bits are well known in the art as evidenced by Stevenson see (Col. 9, Lines 55-57). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Stevenson with Kerth in order to use logic elements such as AND, OR, XOR, XNOR gates to mix and/or combine digital bits to function in desirable manner. Kerth is silent about weighting resistances in series with the outputs of the logic gates for combining the digital representation of the down-converted in-phase and quadrature components according to a value in and in-phase and a quadrature phase signals. Baltus teaches applying weighting resistances in series with the outputs of the digital mixers 20 to the filtered down converted signal and producing intermediate frequency signals IF1-IF4 (Fig. 3; Col. 3, Lines 32-45). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Baltus with Kerth and Stevenson in order to binary weighting the combined signal for forming the intermediate frequency signals IF1-IF4 to provide an accurate quadrature receiver that is low cost and has reduced power consumption (Col. 1, Lines 38-40)\.

Allowable Subject Matter

Claims 9-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As to claims 9-10, the prior art of record fails to teach the limitations cited in the claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Freshteh N. Aghdam whose telephone number is (571) 272-6037. The examiner can normally be reached on Monday through Friday 9:00-5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KEVIN BURD
PRIMARY EXAMINER

Freshteh Aghdam
October 5, 2005